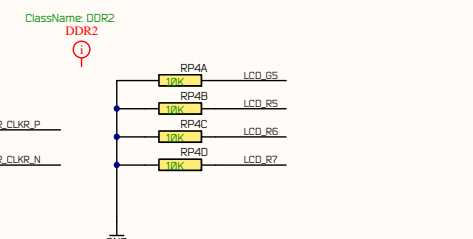
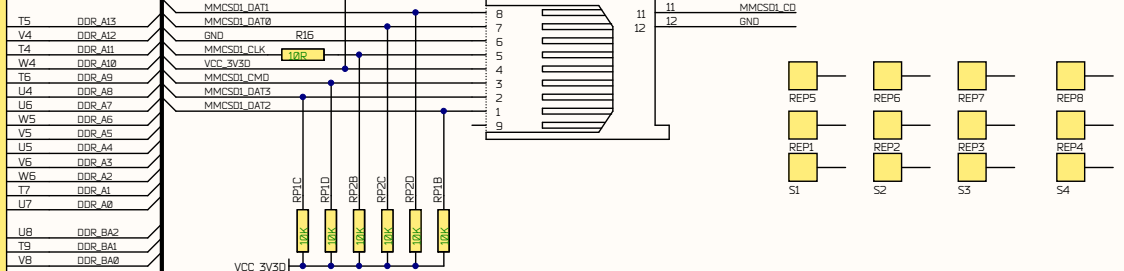
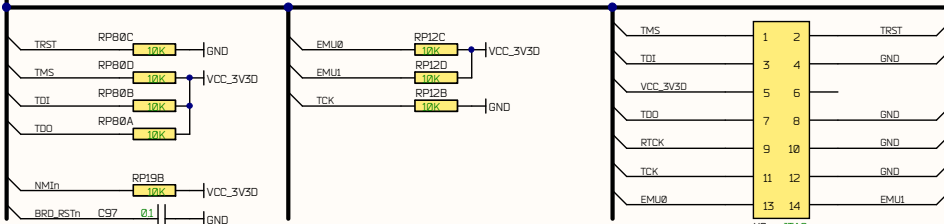
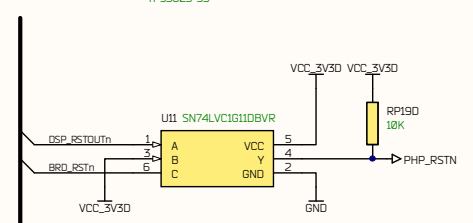
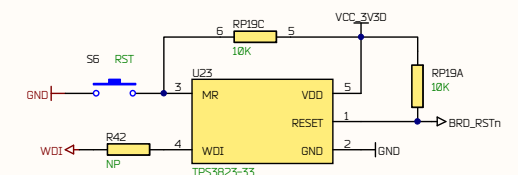
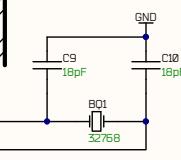
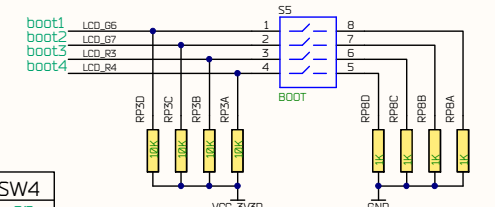


USA OMAP-L138ZWT

MMCS00_CLK	F9	MMCS00_CLK/PRU0_R30[31]/GP4[7]/PRU1_R3[23]	DDR_A[13]	T5	DDR_A13
MMCS00_CMD	A10	EMA_A22/MMCS00_CMD/PRU1_R30[30]/GP4[6]/PRU1_R3[22]	DDR_A[12]	V4	DDR_A12
MMCS00_DAT0	B10	EMA_A21/MMCS00_DAT0/PRU1_R30[29]/GP4[5]/PRU1_R3[21]	DDR_A[11]	T4	DDR_A11
MMCS00_DAT1	A11	EMA_A20/MMCS00_DAT1/PRU1_R30[28]/GP4[4]/PRU1_R3[20]	DDR_A[10]	T6	DDR_A9
MMCS00_DAT2	C10	EMA_A19/MMCS00_DAT2/PRU1_R30[27]/GP4[3]/PRU1_R3[19]	DDR_A[9]	L4	DDR_A8
MMCS00_DAT3	E11	EMA_A18/MMCS00_DAT3/PRU1_R30[26]/GP4[2]/PRU1_R3[18]	DDR_A[8]	U5	DDR_A7
MMCS00_DAT4	B11	EMA_A17/MMCS00_DAT4/PRU1_R30[25]/GP4[1]	DDR_A[7]	W6	DDR_A6
MMCS00_DAT5	E12	EMA_A16/MMCS00_DAT5/PRU1_R30[24]/GP4[0]	DDR_A[6]	L5	DDR_A5
MMCS00_DAT6	C11	EMA_A15/MMCS00_DAT6/PRU1_R30[23]/GP5[15]	DDR_A[5]	V5	DDR_A4
MMCS00_DAT7	A12	EMA_A14/MMCS00_DAT7/PRU1_R30[22]/GP5[14]	DDR_A[4]	W5	DDR_A3
EMA_A13/GP5-13	D11	EMA_A13/PRU0_R30[21]/PRU1_R30[21]/GP5[13]	DDR_A[3]	V6	DDR_A2
EMA_A12/GP5-12	D13	EMA_A12/PRU0_R30[20]/GP5[12]	DDR_A[2]	T7	DDR_A1
EMA_A11/GP5-11	B12	EMA_A11/PRU1_R30[19]/GP5[11]	DDR_A[1]	L7	DDR_A0
EMA_A10/GP5-10	C12	EMA_A10/PRU1_R30[18]/GP5[10]	DDR_A[0]	U8	DDR_BA2
EMA_A9/GP5-9	D12	EMA_A9/PRU1_R30[17]/GP5[9]	DDR_BA[1]	T9	DDR_BA1
EMA_A8/GP5-8	A13	EMA_A8/PRU1_R30[16]/GP5[8]	DDR_BA[0]	V8	DDR_BA0
EMA_A7/GP5-7	B13	EMA_A7/PRU1_R30[15]/GP5[7]	DDR_D[15]	W10	DDR_DR15
EMA_A6/GP5-6	E13	EMA_A6/GP5[5]	DDR_D[14]	L11	DDR_DR14
EMA_A5/GP5-5	C13	EMA_A5/GP5[5]	DDR_D[13]	V10	DDR_DR13
EMA_A4/GP5-4	A14	EMA_A4/GP5[4]	DDR_D[12]	L10	DDR_DR12
EMA_A3/GP5-3	D14	EMA_A3/GP5[3]	DDR_D[11]	T12	DDR_DR11
EMA_A2/NAND_CLE	B14	EMA_A2/GP5[2]	DDR_D[10]	L10	DDR_DR10
EMA_A1/NAND_ALE	D15	EMA_A1/GP5[1]	DDR_D[9]	T11	DDR_DR9
EMA_A0	C14	EMA_A0/GP5[0]	DDR_D[8]	T13	DDR_DR8
EMA_BA1	A15	EMA_BA[1]/GP2[9]	DDR_D[7]	W11	DDR_DR7
EMA_BA0	C15	EMA_BA[0]/GP2[8]	DDR_D[6]	W12	DDR_DR6
EMA_D15	E6	EMA_D[15]/GP3[7]	DDR_D[5]	V12	DDR_DR5
EMA_D14	C7	EMA_D[14]/GP3[6]	DDR_D[4]	V13	DDR_DR4
EMA_D13	B6	EMA_D[13]/GP3[5]	DDR_D[3]	L13	DDR_DR3
EMA_D12	A6	EMA_D[12]/GP3[4]	DDR_D[2]	U14	DDR_DR2
EMA_D11	D6	EMA_D[11]/GP3[3]	DDR_D[1]	L15	DDR_DR1
EMA_D10	A7	EMA_D[10]/GP3[2]	DDR_D[0]	W8	DDR_CLK_P
EMA_D9	D9	EMA_D[9]/GP3[1]	DDR_CLKN	W7	DDR_CLK_N
EMA_D8	E10	EMA_D[8]/GP3[0]	DDR_CKE	V7	DDR_CKE
EMA_D7/NAND_G7	D7	EMA_D[7]/GP4[15]	DDR_CS	V9	DDR_CS
EMA_D6/NAND_D6	C6	EMA_D[6]/GP4[14]	DDR_WE	T8	DDR_WE
EMA_D5/NAND_D5	E7	EMA_D[5]/GP4[13]	DDR_RAS	U9	DDR_RAS
EMA_D4/NAND_D4	B5	EMA_D[4]/GP4[12]	DDR_CAS	W9	DDR_CAS
EMA_D3/NAND_D3	E8	EMA_D[3]/GP4[11]	DDR_DOS[1]	V11	DDR_DOS1
EMA_D2/NAND_D2	B8	EMA_D[2]/GP4[10]	DDR_DOS[0]	T14	DDR_DOS0
EMA_D1/NAND_D1	A8	EMA_D[1]/GP4[9]	DDR_DOGATE0	E11	DDR_DOGATE0
EMA_D0/NAND_D0	C9	EMA_D[0]/GP4[8]	DDR_DOGATE1	R12	DDR_DOGATE1
EMA_CLK	B7	EMA_CLK/PRU0_R30[5]/GP2[7]/PRU0_R3[5]	DDR_DDM[1]	R10	DDR_DDM1
MMCS00_CD	D8	EMA_SDCKE/PRU0_R30[4]/GP2[6]/PRU0_R3[4]	DDR_DDM[0]	W13	DDR_DDM0
EMA_CSN5	B16	EMA_CSN[5]/GP3[12]	USB0_DRVVBUS	K18	USB0DRVBUS
EMA_CSN4	F9	EMA_CSN[4]/GP3[13]	USB0_VBUS	N19	USB0_VCC
NAND_CE	A17	EMA_CSN[3]/GP3[14]	USB0_DM	M18	USB0_D_N
EMA_CSN2	B17	EMA_CSN[2]/GP3[15]	USB0_DP	M19	USB0_D_P
EMA_CSN0	A18	EMA_CSN[0]/GP2[0]	USB0_ID	P16	USB0ID
NAND_WE	B9	EMA_WE/GP3[11]	USB1_DM	P18	USB1_D_N
NAND_RE	B15	EMA_RE/GP3[10]	USB1_DP	P19	USB1_D_P
EMA_RW	D10	EMA_A_RW/GP3[9]	RTC_XI	J18	RTC_XI
GP2-5	A16	EMA_RAS/PRU0_R30[3]/GP2[5]/PRU0_R3[3]	RTC_XO	H19	RTC_XO
USB1DRVBUS	A9	EMA_CAS/PRU0_R30[2]/GP2[4]/PRU0_R3[2]	OSCIN	L19	OSCIN
GP2-2	A5	EMA_WEN_DOM[1]/GP2[2]	OSCOUT	K19	OSCOUT
GP2-3	C8	EMA_WEN_DOM[0]/GP2[3]			
EMA_WAIT1	B19	EMA_WAIT[1]/PRU0_R30[11]/GP2[1]/PRU0_R3[11]			
NAND_RB	B18	EMA_WAIT[0]/PRU0_R30[10]/GP2[0]/PRU0_R3[10]			
TDI	M16				
TDO	J18				
TMS	L16				
TCK	J15				
TRST	L17				
EMUJ1	K16				
EMUJ0	J16				
RTCK	K17				
NMIn	J17				
DSP_RSTOUTn	T17				
BRD_RSTn	K14				
AMCLK	T18				



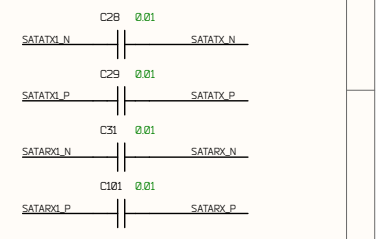
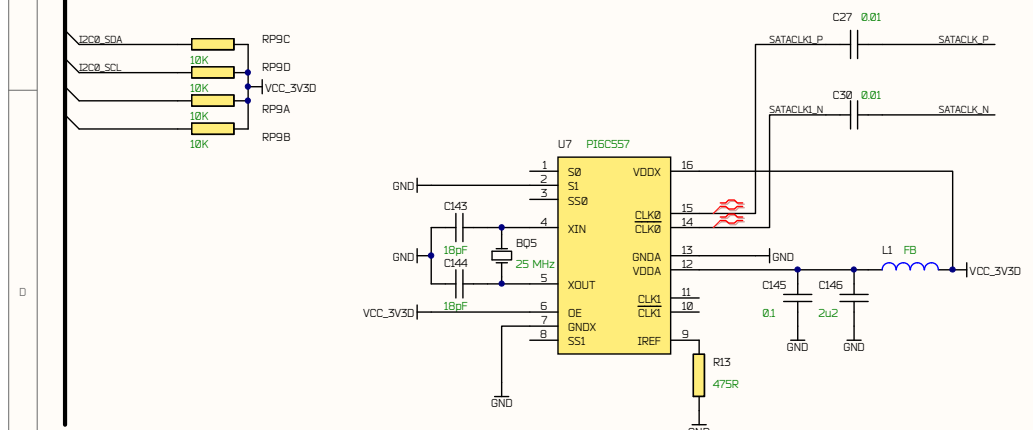
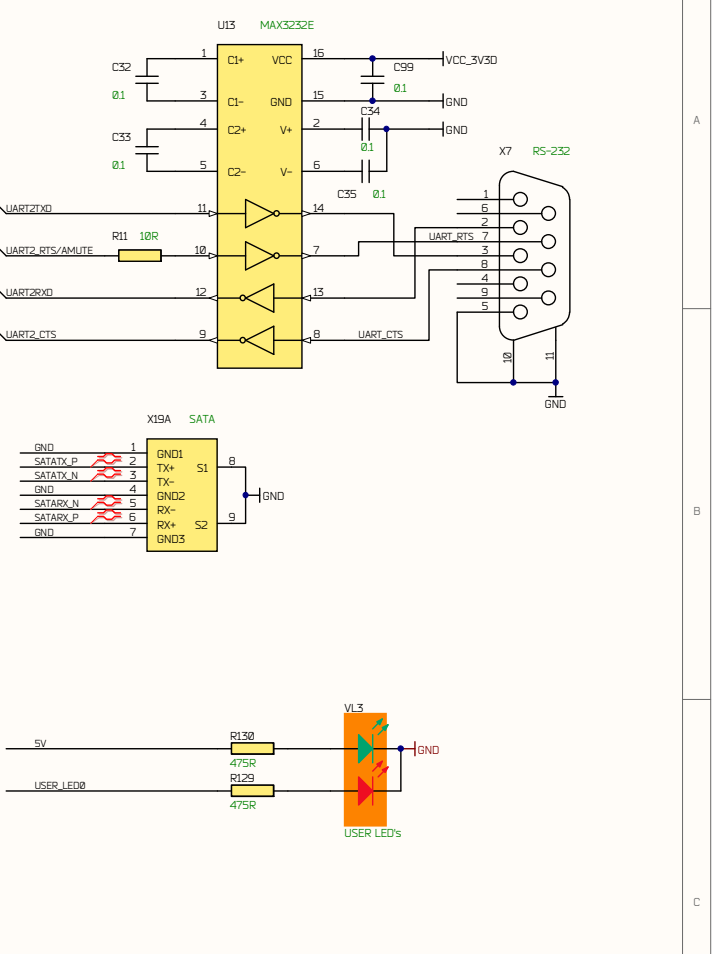
SOURCE	SW1	SW2	SW3	SW4
NAND 8-bit	off	off	off	on
SPI1 FLASH	on	off	off	on
UART2	on	off	on	off



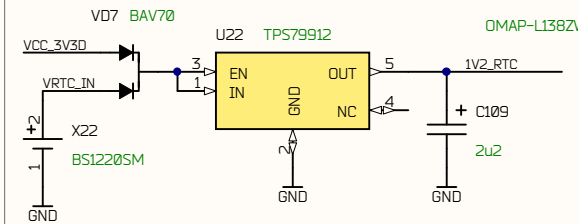
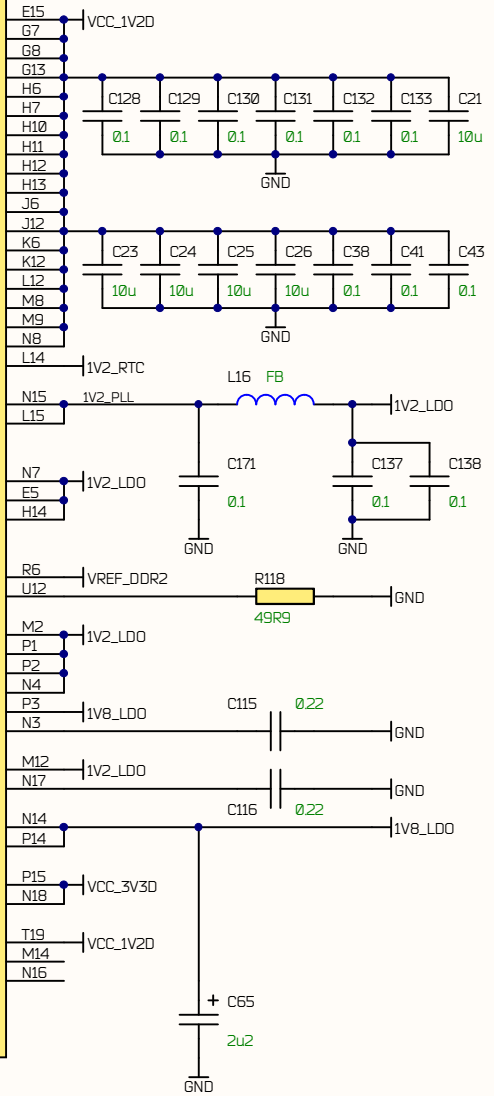
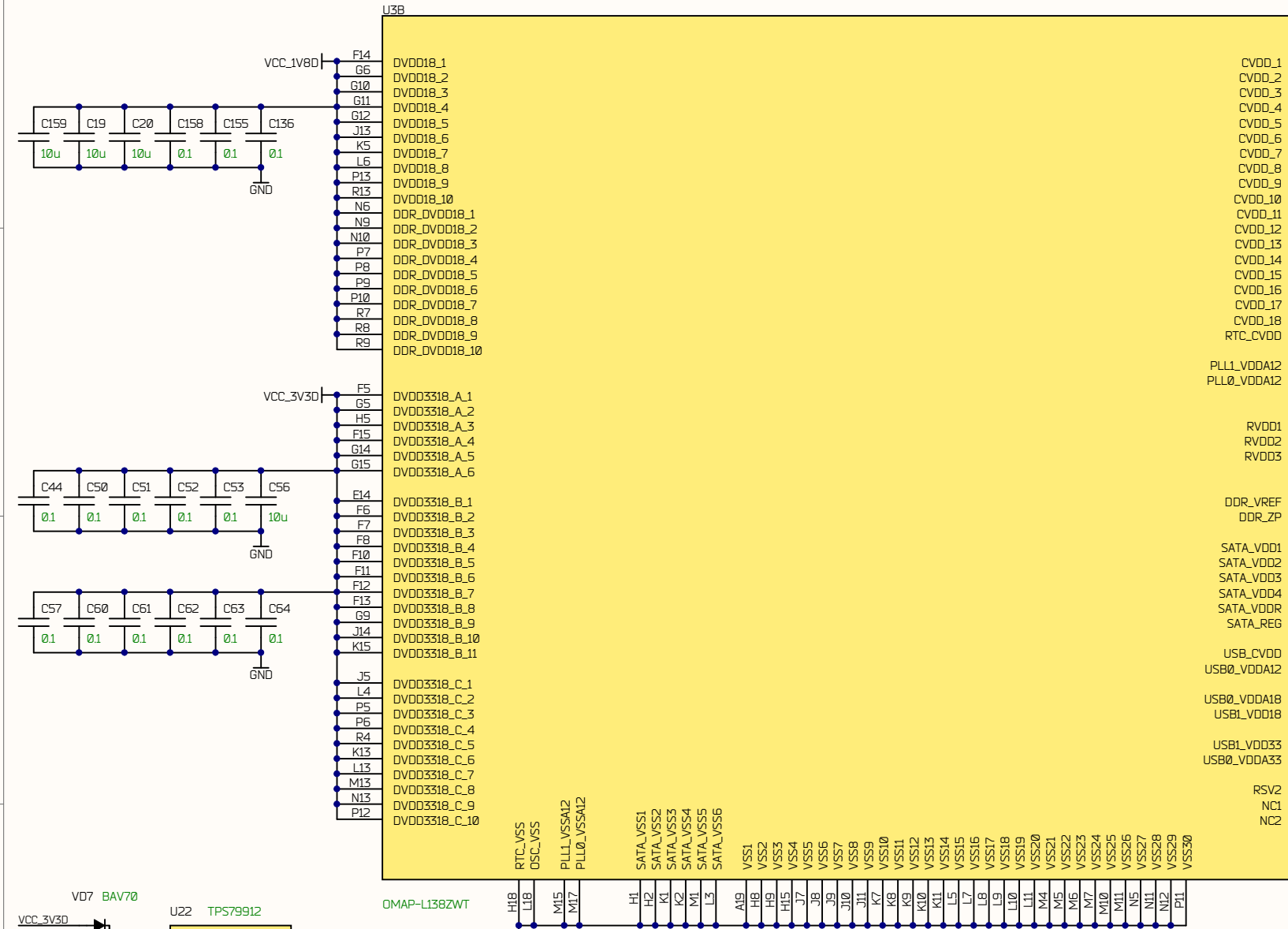
Title			
Size	Number	Revision	
A3			
Date:	23.11.2012	Sheet of	
File:	D:\My_work\evam1808_cpuchdco	Drawn By:	

U3C OMAP-L138ZWT

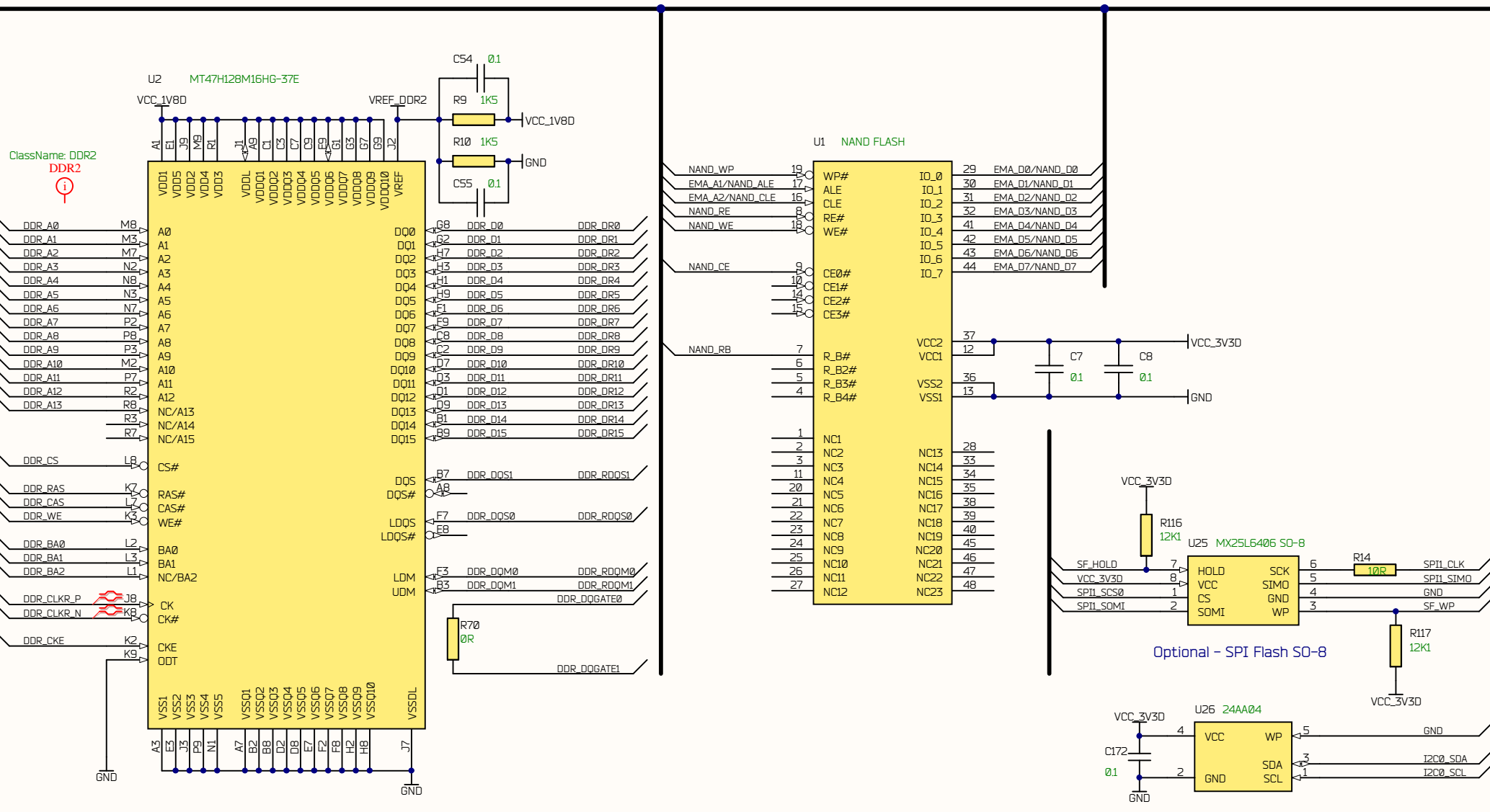
VP_DIN7	V18	VP_DIN[15]_VSYNC/UHPT_HD[7]/APP_D[7]/PRU0_R30[15]/PRU0_R31[15]	VP_DOUT[15]/LCD_D[5]/APP_XD[7]/GP[7]/B00T[7]	P4	LCD_B7
VP_DIN6	V19	VP_DIN[14]_HSYNC/UHPT_HD[6]/APP_D[6]/PRU0_R30[14]/PRU0_R31[14]	VP_DOUT[14]/LCD_D[4]/APP_XD[6]/GP[6]/B00T[6]	R3	LCD_B6
VP_DIN5	U19	VP_DIN[13]_FIELD/UHPT_HD[5]/APP_D[5]/PRU0_R30[13]/PRU0_R31[13]	VP_DOUT[13]/LCD_D[3]/APP_XD[5]/GP[5]/B00T[5]	R2	LCD_B5
VP_DIN4	T16	VP_DIN[12]/UHPT_HD[4]/APP_D[4]/PRU0_R30[12]/PRU0_R31[12]	VP_DOUT[12]/LCD_D[2]/APP_XD[4]/GP[4]/B00T[4]	R1	LCD_B4
VP_DIN3	R18	VP_DIN[11]/UHPT_HD[3]/APP_D[3]/PRU0_R30[11]/PRU0_R31[11]	VP_DOUT[11]/LCD_D[1]/APP_XD[3]/GP[3]/B00T[3]	T3	LCD_B3
VP_DIN2	R19	VP_DIN[10]/UHPT_HD[2]/APP_D[2]/PRU0_R30[10]/PRU0_R31[10]	VP_DOUT[10]/LCD_D[0]/APP_XD[2]/GP[2]/B00T[2]	T2	LCD_B2
VP_DIN1	R15	VP_DIN[9]/UHPT_HD[1]/APP_D[1]/PRU0_R30[9]/PRU0_R31[9]	VP_DOUT[9]/LCD_D[0]/APP_XD[1]/GP[1]/B00T[1]	T1	LCD_B1
VP_DIN0	P17	VP_DIN[8]/UHPT_HD[0]/APP_D[0]/GP[8]/PRU1_R31[8]	VP_DOUT[8]/LCD_D[0]/APP_XD[0]/GP[7]/B00T[7]	U5	LCD_B0
ETH_TXD	U18	VP_DIN[7]/UHPT_HD[0]/APP_D[0]/RMIL_TXD[0]/PRU0_R31[29]	VP_DOUT[7]/LCD_D[7]/APP_XD[15]/PRU1_R31[15]	U2	LCD_B4
ETH_TXD0	V16	VP_DIN[6]/UHPT_HD[0]/APP_D[0]/RMIL_TXD[0]/PRU0_R31[28]	VP_DOUT[6]/LCD_D[6]/APP_XD[14]/GP[14]/PRU1_R31[14]	U1	LCD_B3
ETH_TXEN	R14	VP_DIN[5]/UHPT_HD[1]/APP_D[1]/RMIL_TXEN/PRU0_R31[27]	VP_DOUT[5]/LCD_D[5]/APP_XD[13]/PRU1_R31[13]	V2	LCD_B7
ETH_RXD1	W16	VP_DIN[4]/UHPT_HD[2]/APP_D[2]/RMIL_RXD[1]/PRU0_R31[26]	VP_DOUT[4]/LCD_D[4]/APP_XD[12]/GP[12]/PRU1_R31[12]	V1	LCD_B6
ETH_RXD0	V17	VP_DIN[3]/UHPT_HD[2]/APP_D[2]/RMIL_RXD[0]/PRU0_R31[25]	VP_DOUT[3]/LCD_D[3]/APP_XD[11]/GP[11]/PRU1_R31[11]	W3	LCD_B5
ETH_RXER	W17	VP_DIN[2]/UHPT_HD[3]/APP_D[3]/RMIL_RXER/PRU0_R31[24]	VP_DOUT[2]/LCD_D[2]/APP_XD[10]/GP[10]/PRU1_R31[10]	U4	LCD_B3
ETH_S0MHz	W18	VP_DIN[1]/UHPT_HD[3]/APP_D[3]/RMIL_MHZ_S0_CLK/PRU0_R31[23]	VP_DOUT[1]/LCD_D[1]/APP_XD[9]/GP[9]/PRU1_R31[9]	W2	LCD_B4
ETH_CRS0V	W19	VP_DIN[0]/UHPT_HD[3]/APP_D[3]/RMIL_CRS_DV/PRU0_R31[22]	VP_DOUT[0]/LCD_D[0]/APP_XD[8]/GP[8]/PRU1_R31[8]	W1	LCD_B3
MMCS0L_DAT1	J3	VP_CLKIN2/MMCS0L_DAT[1]/PRU1_R30[1]/GP[6]/PRU1_R31[2]	MMCS0L_DAT[5]/LCD_HSYNC/PRU1_R30[5]/GP[8]/PRU1_R31[6]	H4	VPIF_HSNCR
MMCS0L_DAT3	H3	VP_CLKIN2/MMCS0L_DAT[3]/PRU1_R30[3]/GP[6]/PRU1_R31[4]	MMCS0L_DAT[4]/LCD_VSYNC/PRU1_R30[4]/GP[8]/PRU1_R31[5]	G4	VPIF_VSNCR
VP_CLK1	V15	VP_CLKIN0/UHPT_HDS1/PRU1_R30[9]/GP[6]/PRU1_R31[16]	MMCS0L_DAT[6]/LCD_MCLK/PRU1_R30[6]/GP[8]/PRU1_R31[7]	F2	DISP_ON
UHP_ZX_TXCLK	W14	VP_CLKIN0/UHPT_HCS/PRU1_R30[10]/GP[6]/PRU1_R31[17]	MMCS0L_DAT[7]/LCD_PCLK/PRU1_R30[7]/GP[8]	F1	VPIF_PCLKR
SPI0_CLK	D19	SPI0_CLK/EPWM0A/GP1[8]/MIL_RXCLK	LCD_AC_ENB_CS/GP[8]/PRU1_R31[28]	R5	VPIF_AC_ENBR
SPI0_S0M1	C16	SPI0_S0M1/EPWM0A/GP1[8]/MIL_RXER	VP_CLKOUT3/PRU1_R30[10]/GP[6]/PRU1_R31[1]	K4	TS_INT
SPI0_S1M0	C18	SPI0_S1M0/EPWM0A/GP1[8]/MIL_RXCRS	VP_CLKOUT2/MMCS0L_DAT[2]/PRU1_R30[2]/GP[3]/PRU1_R31[3]	K3	MMCS0L_DAT2
SPI0_ENA	C17	SPI0_ENA/EPWM0B/PRU0_R30[6]/MIL_RXD0V	PRU0_R30[25]/MMCS0L_DAT[0]/APP_CHB_CLOCK/GP[15]/PRU1_R31[27]	G1	MMCS0L_DAT8
UART0_RXD	C19	SPI0_SCS[5]/UART0_RXD/GP[8]/MIL_RXD[3]	PRU0_R30[24]/MMCS0L_CLK/APP_CHB_START/GP[15]/PRU1_R31[26]	G2	MMCS0L_CLK
UART0_TXD	D18	SPI0_SCS[4]/UART0_TXD/GP[8]/MIL_RXD[2]	PRU0_R30[23]/MMCS0L_CMD/APP_CHB_ENABLE/GP[15]/PRU1_R31[25]	J4	MMCS0L_CMD
UART0_CTS	E17	SPI0_SCS[3]/UART0_CTS/GP[8]/MIL_RXD[1]	PRU0_R30[22]/PRU1_R30[8]/APP_CHB_WAIT/GP[15]/PRU1_R31[24]	G3	GP8-I2
UART0_RTS	D16	SPI0_SCS[2]/UART0_RTS/GP[8]/MIL_RXD[0]/SATA_MP_SWITCH	PRU0_R30[29]/UHPT_HCNTL0/APP_CHA_CLOCK/GP[11]	U17	UHP_CHA_CLK
ETH_MDC	E16	SPI0_SCS[1]/TM64P0_OUT12/GP1[7]/MDC0_CLK/TM64P0_IN12	PRU0_R30[28]/UHPT_HCNTL1/APP_CHA_START/GP[10]	W15	UHP_CHA_START
ETH_MDIO	D17	SPI0_SCS[0]/TM64P1_OUT12/GP1[6]/MDIO_D/TM64P1_IN12	PRU0_R30[27]/UHPT_HHWL/APP_CHA_ENABLE/GP[9]	U16	UHP_CHA_EN
SPI1_CLK	G19	SPI1_CLK/GP2[15]	PRU0_R30[26]/UHPT_HRW/APP_CHA_WAIT/GP[8]/PRU1_R31[17]	T15	UAPP_CHA_WAI
SPI1_S0M1	H17	SPI1_S0M1/GP2[11]	PRU0_R30[30]/UHPT_HINT/PRU1_R30[11]/GP[6]	R16	GP6-I2
SPI1_S1M0	G17	SPI1_S1M0/GP2[10]	PRU0_R30[31]/UHPT_HRDY/PRU1_R30[12]/GP[6]	R17	UHPT_HRDY
SPI1_ENA	H16	SPI1_ENA/GP2[12]	AXR6/CLKR0/GP1[4]/MIL_TXEN/PRU0_R31[6]	D1	MCASP_AXR6
I2C0_SCL	G16	SPI1_SCS[7]/I2C0_SCL/TM64P2_OUT12/GP1[5]	AXR5/CLKR0/GP1[5]/MIL_TXCLK	C3	MCASP_AXR5
I2C0_SDA	G18	SPI1_SCS[6]/I2C0_SDA/TM64P3_OUT12/GP1[4]	AXR0/ECAP0_APWM0/GP[7]/MIL_TXD[0]/MIL_D0L	F3	MCASP_AXR0
UART2RXD	F17	SPI1_SCS[5]/UART2_RXD/I2CL_SCL/GP1[3]	AXR4/FSR0/GP1[2]/MIL_D0L	D1	MCASP_AXR4
UART2TXD	F16	SPI1_SCS[4]/UART2_TXD/I2CL_SDA/GP1[2]	AXR3/FSX0/GP1[1]/MIL_TXD[5]	E3	MCASP_AXR3
UART1_RXD	E18	SPI1_SCS[3]/UART1_RXD/SATA_LED/GP1[1]	AXR2/DR0/GP1[1]/MIL_TXD[2]	E2	MCASP_AXR2
UART1_TXD	F19	SPI1_SCS[2]/UART1_TXD/SATA_CP_POD/GP1[0]	AXR1/DR0/GP1[9]/MIL_TXD[1]	E1	MCASP_AXR1
SPI1_SCS1	F18	SPI1_SCS[1]/EPWM1A/PRU0_R30[7]/GP2[15]/TM64P2_IN12	AXR14/CLKR1/GP[8]	B4	AIC_BCLK
SPI1_SCS0	E19	SPI1_SCS[0]/EPWM1B/PRU0_R30[8]/GP2[14]/TM64P3_IN12	AXR13/CLKL1/GP[8]	B3	INTn
UART2_CTS	F4	RSVD/RTC_ALARM/UART2_CTS/GP[8]/DEEPSLEEP	AXR8/CLKS1/ECAP1_APWM1/GP[8]/PRU0_R31[8]	E4	APWM1
UART2_RTS/AMUTE	D5	AMUTE/PRU0_R30[16]/UART2_RTS/GP[8]/PRU0_R31[16]	AXR12/FSX1/GP[9]	C5	USER_LED0
MCASP_AXR7	D2	AXR7/EPWM17[20]/PRU0_R30[17]/GP1[15]/PRU0_R31[7]	AXR11/FSX1/GP[9]	C4	AIC_WCLK
GP0-7	A4	AXR5/EPWM0[70]/ECAP2_APWM2/GP[7]	AXR10/DR1/GP[2]	D4	AIC_DOUT
MCASP_FSK	B2	AIFS/GP[0][2]/PRU0_R31[9]	AXR9/DX1/GP[0][1]	C3	AIC_DIN
MCASP_FSR	C2	AFSR/GP[0][3]/PRU0_R31[20]	SATA_REFCLK	N1	SATACKL_N
UART1_CTS/AHCLK	A3	AHCLK/USB_REFCLKIN/UART1_CTS/GP[0][10]/PRU0_R31[7]	SATA_REFCLKP	N2	SATACKL_P
UART1_RTS/AHCLK	A2	AHCLKR/PRU0_R30[18]/UART1_RTS/GP[0][11]/PRU0_R31[18]	SATA_TXN	J2	SATATX1_N
MCASP_CLKX	B1	ACLKX/PRU0_R30[9]/GP[14]/PRU0_R31[21]	SATA_TXP	J1	SATATX1_P
MCASP_CLKR	A1	ACLKR/PRU0_R30[20]/GP[0][15]/PRU0_R31[22]	SATA_RXN	L2	SATARX1_N
			SATA_RXP	L1	SATARX1_P
			NCS	M3	



Title		
Size	Number	Revision
A3		
Date:	23.11.2012	Sheet of
File:	D:\My_work\...\evam1808_interfaceschd\Drawn By:	



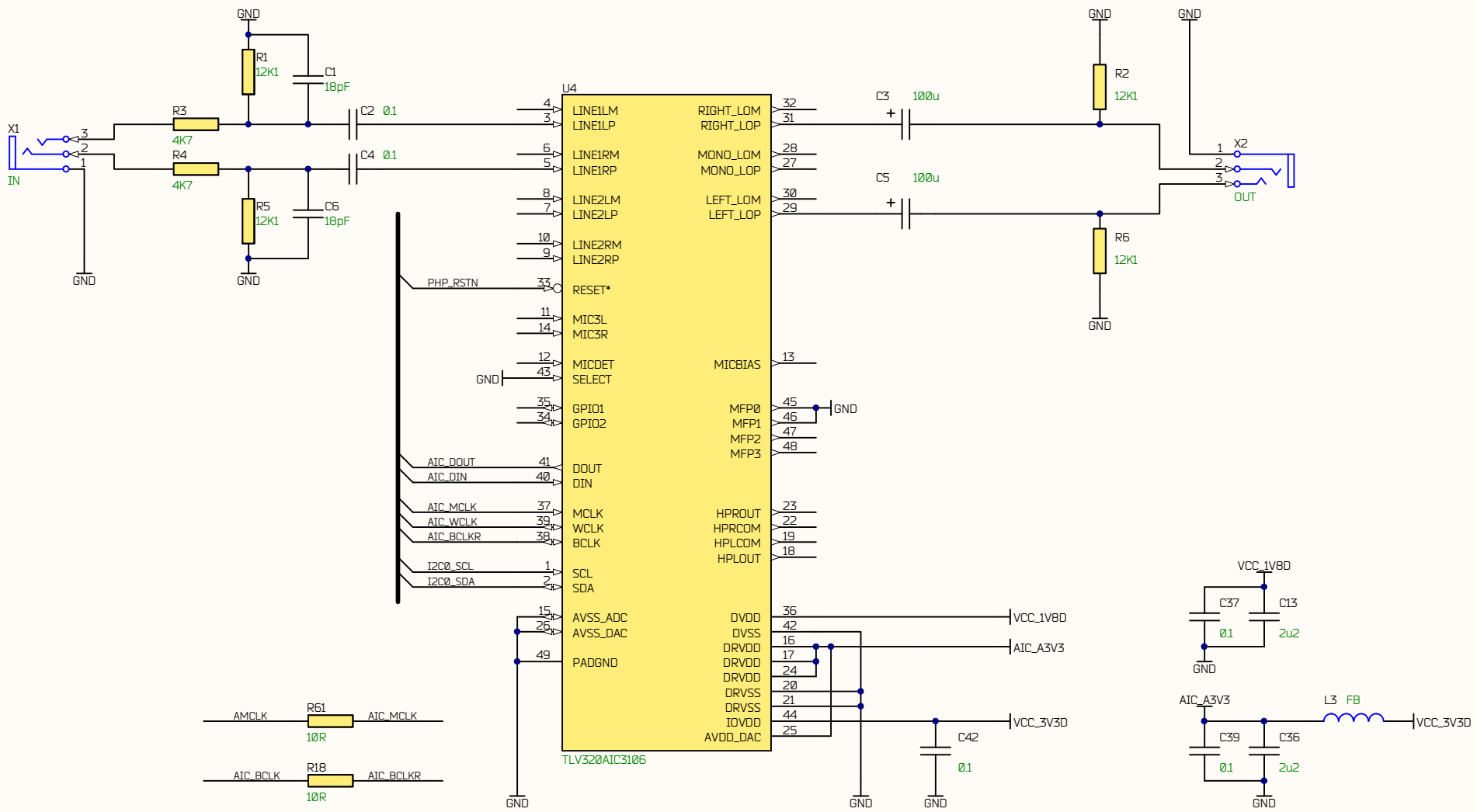
Title		
Size	Number	Revision
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File:	D:\My_work\levam1808_connectors.sch	
	Drawn By:	



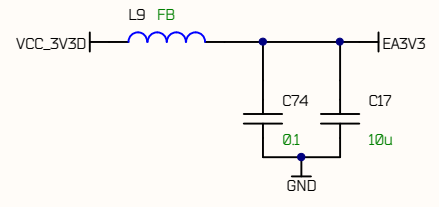
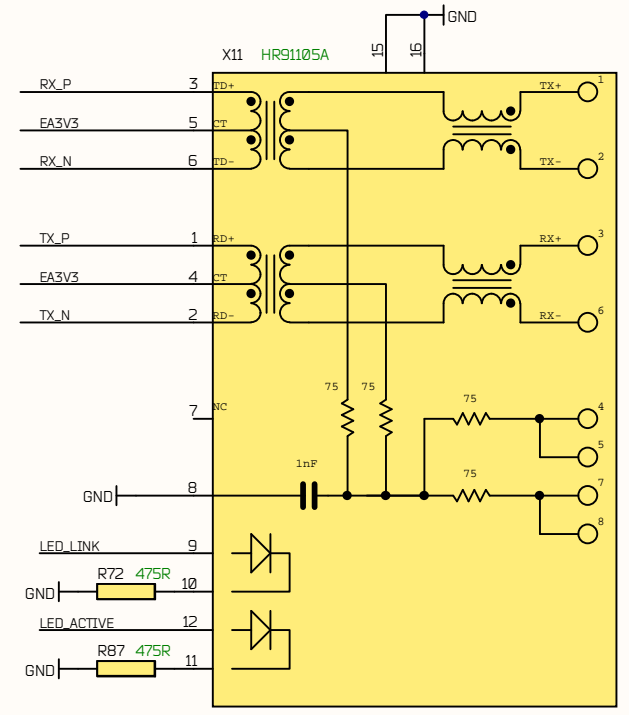
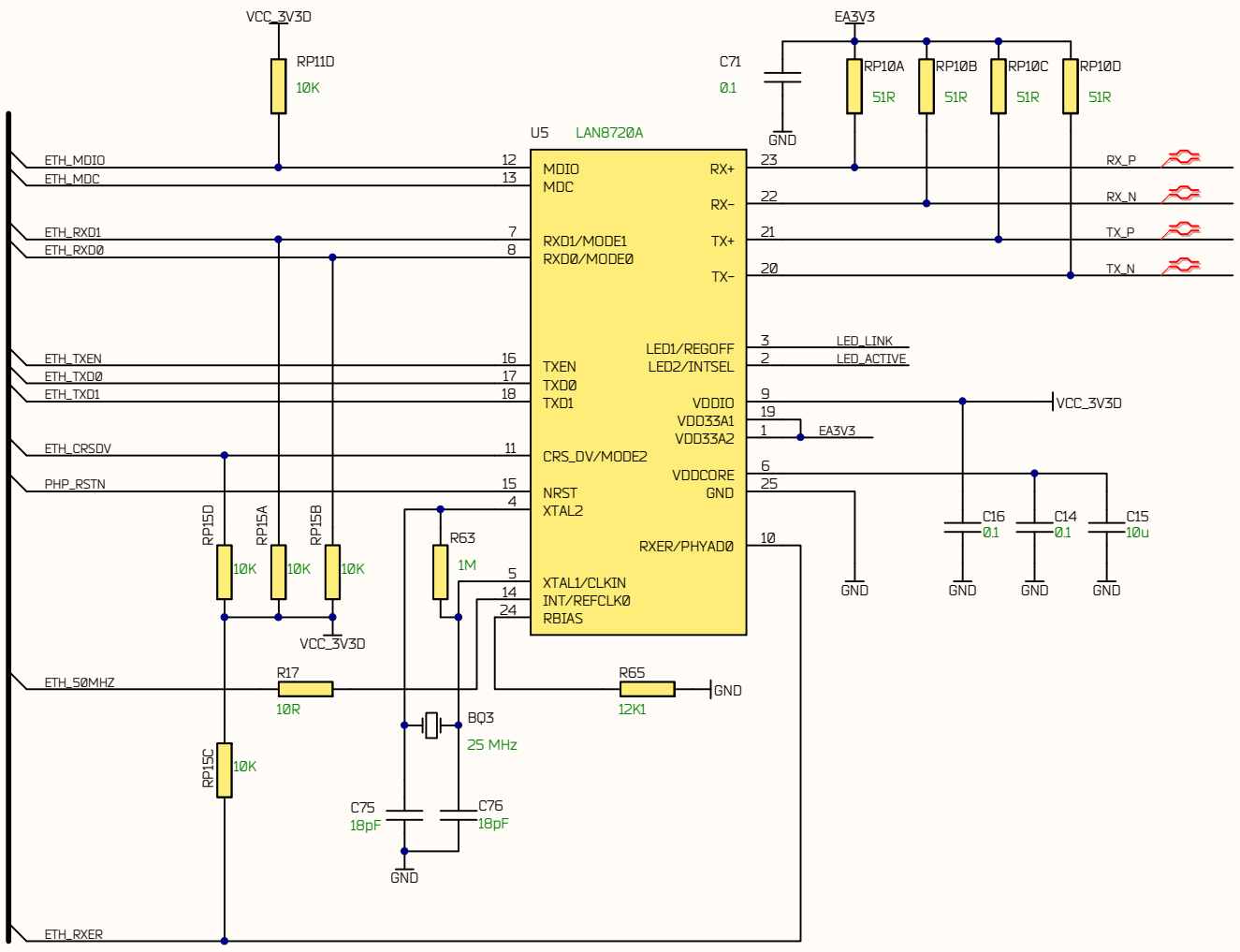
Optional - SPI Flash SO-8

Optional - I2C EEPROM

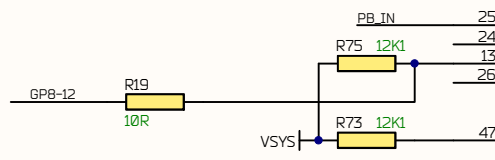
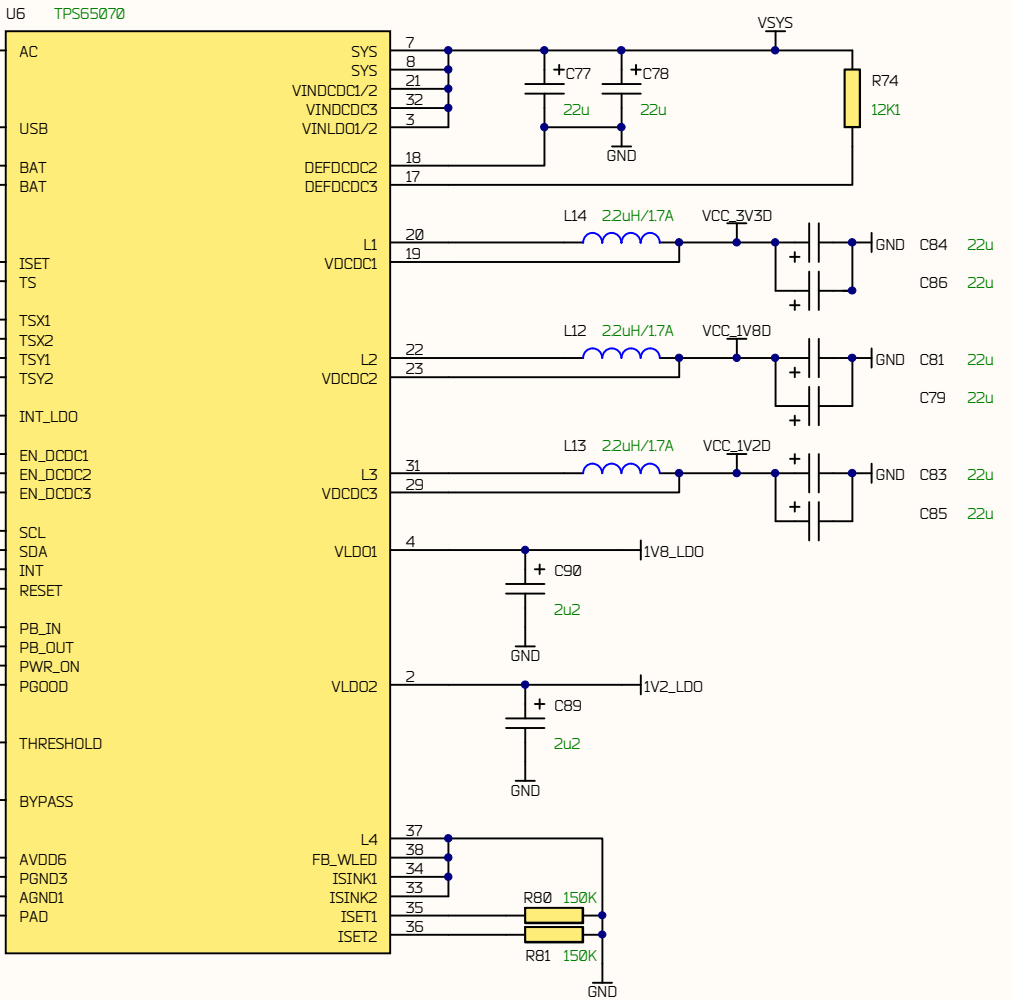
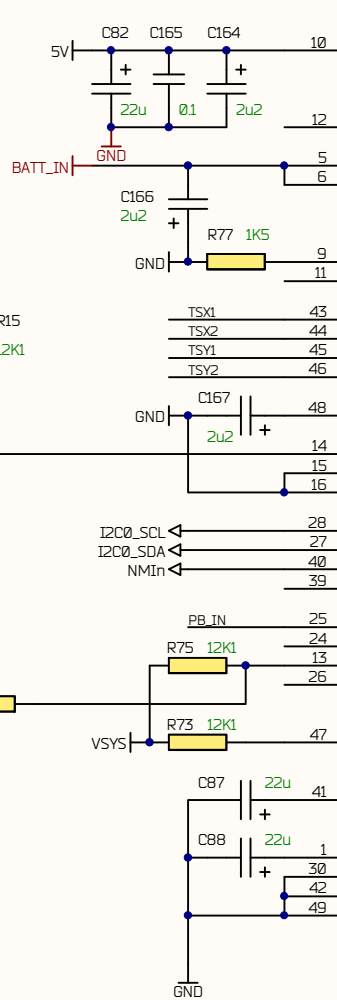
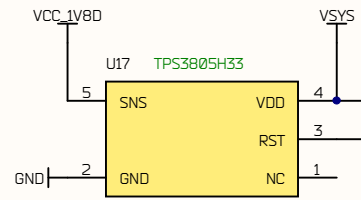
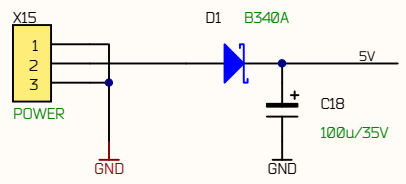
Title		
Size	Number	Revision
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File:	D:\My_work\levam1008_memory.schdoc	Drawn By:



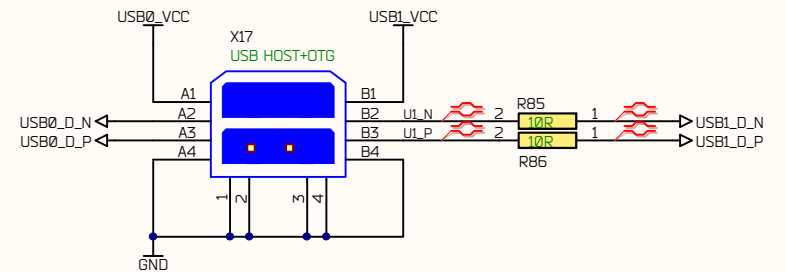
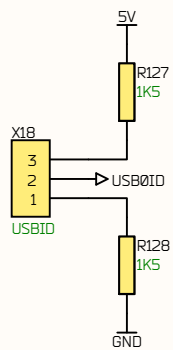
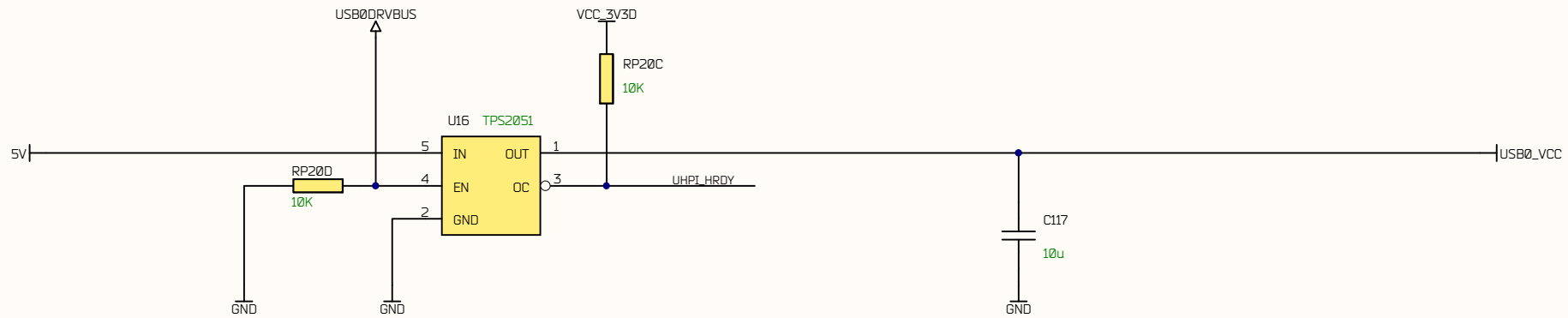
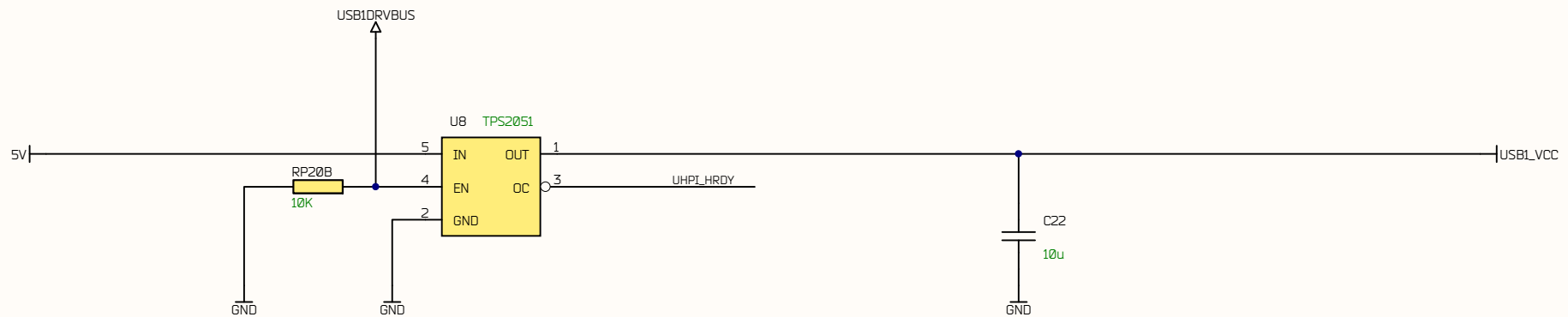
Title		
Size	Number	Revision
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File:	D:\My_work\levam1008_audio.schdoc	Drawn By:



Title		
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File:	D:\My_work\levam1008_ethernet.schddc Drawn By:	



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File:	D:\My_work\levam1008_power.schdoc	Drawn By:



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GND	1	2	GND
EMA_D15	3	4	EMA_D14
EMA_D13	5	6	EMA_D12
EMA_D11	7	8	EMA_D10
EMA_D9	9	10	EMA_D8
EMA_D7/NAND_D7	11	12	EMA_D6/NAND_D6
EMA_D5/NAND_D5	13	14	EMA_D4/NAND_D4
EMA_D3/NAND_D3	15	16	EMA_D2/NAND_D2
EMA_D1/NAND_D1	17	18	EMA_D0/NAND_D0
GND	19	20	GND
EMA_A13/GP5-13	21	22	EMA_A12/GP5-12
EMA_A11/GP5-11	23	24	EMA_A10/GP5-10
EMA_A9/GP5-9	25	26	EMA_A8/GP5-8
EMA_A7/GP5-7	27	28	EMA_A6/GP5-6
EMA_A5/GP5-5	29	30	EMA_A4/GP5-4
EMA_A3/GP5-3	31	32	EMA_A2/NAND_CLE
EMA_A1/NAND_ALE	33	34	EMA_A0
EMA_BA1	35	36	EMA_BA0
EMA_CSN5	37	38	EMA_CSN4
VCC_3V3D	39	40	NAND_WE
NAND_RE	41	42	EMA_RW
EMA_CSN2	43	44	EMA_CSN0
EMA_WAIT1	45	46	EMA_CLK
GND	47	48	GND
SPI0_ENA	49	50	SPI0_SIMO
SPI0_CLK	51	52	SPI0_SOMI
SPI1_ENA	53	54	VCC_3V3D
SPI1_CLK	55	56	SPI1_SOMI
SPI1_SCS1	57	58	SPI1_SIMO

CONN

UPP_2X_TXCLK	1	2	UPP_CHA_EN
UPP_CHA_CLK	3	4	UAPP_CHA_WAIT
UPP_CHA_START	5	6	5V
I2C0_SDA	7	8	I2C0_SCL
PHP_RSTN	9	10	
VP_DIN0	11	12	VP_DIN1
VP_DIN2	13	14	VP_DIN3
VP_DIN4	15	16	VP_DIN5
VP_DIN6	17	18	VP_DIN7
GND	19	20	VCC_3V3D

VIDEO IN

5V	1	2	GND
I2C0_SCL	3	4	I2C0_SDA
GP2-5	5	6	GP2-2
GP0-7	7	8	GP2-3
VCC_3V3D	9	10	GND
MMCSDB0_CLK	11	12	MMCSDB0_CMD
MMCSDB0_DAT0	13	14	MMCSDB0_DAT1
MMCSDB0_DAT2	15	16	MMCSDB0_DAT3
MMCSDB0_DAT4	17	18	MMCSDB0_DAT5
MMCSDB0_DAT6	19	20	MMCSDB0_DAT7

VIDEO IN

TS_INT	1	2	DISP_ON
TSX1	3	4	TSY1
TSX2	5	6	TSY2
VCC_3V3D	7	8	5V
GND	9	10	GND
VPIF_VSYNCR	11	12	VPIF_PCLKR
VPIF_AC_ENBR	13	14	VPIF_HSYNCR
LCD_B4	15	16	LCD_B3
LCD_B6	17	18	LCD_B5
LCD_G2	19	20	LCD_B7
LCD_G4	21	22	LCD_G3
LCD_G6	23	24	LCD_G5
LCD_R3	25	26	LCD_G7
LCD_R5	27	28	LCD_R4
LCD_R7	29	30	LCD_R6

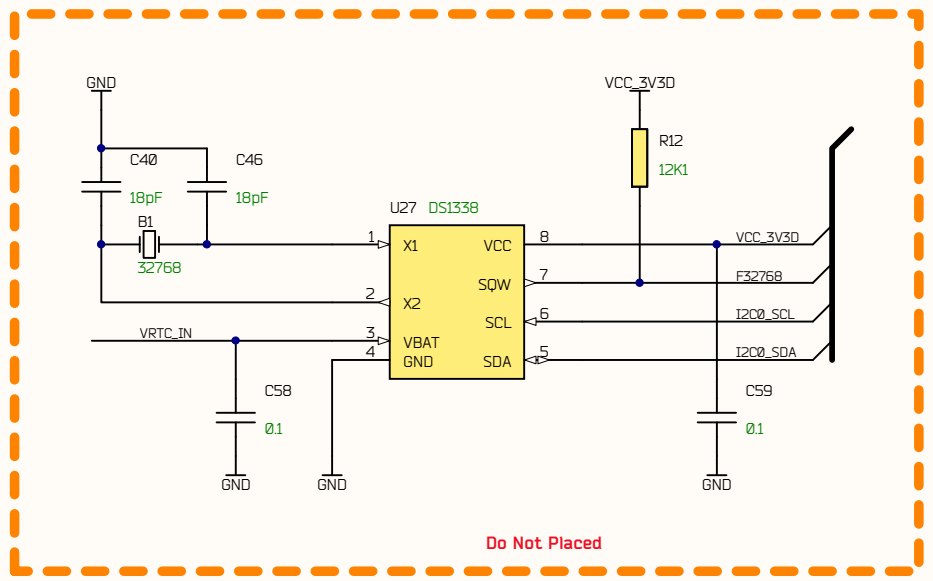
VIDEO OUT

GND	1	2	GND
MCASP_AXR0	3	4	MCASP_AXR3
MCASP_AXR2	5	6	MCASP_AXR1
MCASP_AXR5	7	8	MCASP_AXR7
MCASP_AXR4	9	10	MCASP_FSR
MCASP_AXR6	11	12	MCASP_FSX
MCASP_CLKX	13	14	MCASP_CLKR
UART1_CTS/AHCLKX	15	16	UART1_RTS/AHCLKR
UART2_RTS/AMUTE	17	18	5V
GND	19	20	VCC_3V3D

VIDEO IN

UART0_RXD	1	2	UART0_TXD
UART0_CTS	3	4	UART0_RTS
5V	5	6	GND
UART1_RXD	7	8	UART1_TXD
UART1_CTS/AHCLKX	9	10	UART1_RTS/AHCLKR
I2C0_SCL	11	12	I2C0_SDA
PB_IN	13	14	
INTn	15	16	PHP_RSTN
APWM1	17	18	GP0-12
GND	19	20	VCC_3V3D

VIDEO IN



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